In the Specification:

Please amend the paragraph at **page 1, lines 4 to 5**, as follows:

The present invention relates to a method for testing an integrated circuit ~~in accordance with the preamble of patent claim 1~~ and a circuit arrangement for performing this method.

Please amend the paragraph at **page 2, lines 11 to 13**, as follows:

~~The first named object of the invention is solved by the features described in patent claim 1. The circuit arrangement is described by the features of patent claims 10 and 11. Favorable embodiments are the objects of the subclaims.~~ The above objects have been achieved according to the invention in a circuit arrangement and a method of operating it, as defined in the claims.

Please amend the paragraph at **page 2, lines 15 to 25**, as follows:

Accordingly, the essence of the invention lies in switching the signals generated by a circuit unit within an integrated circuit, which are not measurable at the outputs in the normal operating mode, as test signals to the existing signal outputs for function checks. To do this, a defined potential value is applied to at least one signal output of the integrated circuit while the supply voltage is available, and the integrated circuit is thus switched into a test mode. A test signal generated by a circuit unit of the integrated circuit is thus applied at the

signal output. In order to be able to achieve a reliable switchover into the test mode, it is necessary for the potential value applied at the signal output to be different ~~to~~ from the value of the output voltage available at the signal output in normal operation of the integrated circuit. It is particularly advantageous if the potential value is applied or set at the signal output by means of a passive component, for example by a resistor.

Please amend the paragraph at **page 3, lines 22 to 25**, as follows:

In the case of a plurality of signal outputs, it is possible in a development of the method for the control unit to test the potential value set at ~~the~~ a first signal output and apply the test signal at another, e.g. second, signal output. The advantages of this are that there is no superimposition with the set direct voltage value and that a direct voltage offset of the test signal can be measured.

Please amend the paragraph at **page 4, lines 5 to 14**, as follows:

In a further development of the method according to the invention, the integrated circuit is switched into the test mode if the potential value available at the signal output of the integrated circuit lies within ~~an~~ a voltage interval of a voltage window discriminator. In so doing, it is advantageous if the signal heights of the test signals, that is their amplitudes and their direct voltage offsets, are set by means of signal amplifiers so that the direct voltage offset of the respective test signal corresponds to

the potential value set at the signal output, and the maximum amplitude of the test signal lies within the interval defined by the respective window discriminator. Crosstalk between adjacent windows of the discriminators can be prevented in this way provided that a plurality of window discriminators are used. Furthermore, the direct voltage value at the signal output is little changed.

Please amend the paragraph at **page 4, lines 28 to 29**, as follows:

Fig. 1 A first circuit arrangement for implementing the method according to the invention, ~~and~~

Please amend the paragraph at **page 4, lines 31 to 32**, as follows:

Fig. 2 A second circuit arrangement for implementing the method according to the invention~~.~~, and

Please insert a new paragraph at **page 4, above existing numbered line 35**, as follows:

Fig. 3 A third circuit arrangement with plural output pins.

Please amend the paragraph at **page 5, lines 8 to 23**, as follows:

There are two functional units within the integrated circuit IC. The first functional unit contains the circuit functions needed for normal operation of the integrated circuit, which are represented, with the exception of a load element RL connected as a "pull up" between the voltage VDD and a node 50, by a circuit unit SCH, the

second functional unit comprises the test mode detection which consists of a control unit ST and a first and a second voltage-controlled switching element E1 and E2. The ~~switching~~ circuit unit or element SCH has a first input which is linked to the signal input IN of the integrated circuit IC, and a second input at which a signal MS is available, and a first output line which is linked to the control unit ST, a second output line which is linked to the switching element E1, at which a signal SW1 which is to be tested is available, and a third output line which is linked to the switching element E2, at which a signal SW2 which is to be tested is available. The circuit unit includes plural internal circuit blocks CB1 and CB2, which may respectively provide the signals SW1 and SW2. The outputs of the two switching elements E1 and E2 are linked to the node 50. Furthermore, the node 50 is linked to the signal output OUT of the integrated circuit IC and by a ~~wire~~ conductor 5 to the control unit ST. The control unit ST has a first output, at which the signal MS is available, which is linked to a control input of the switching element E1 and to the second input of the circuit unit SCH, and a second output which is linked to a control input of the switching element E2.

Please amend the paragraph at **page 6, line 12 to page 7, line 11**, as follows:

The object of the integrated circuit IC shown in figure 2 is to supply an alternating voltage signal in normal

operation. Whereas the external wiring of the integrated circuit IC is identical with the embodiment illustrated in figure 1, an advantageous implementation of a control unit ST is presented in a further development of the embodiment in figure 1. In the embodiment illustrated, the switchover of the integrated circuit into the test mode is a function of the result of a logical operation of the set potential value and the control signal of an output stage of the integrated circuit IC. The input IN is linked to a first input of a ~~switching~~ circuit element SCH1 within the integrated circuit IC. Furthermore, the ~~switching~~ circuit element SCH1 has a second input at which a signal MS is available, and a first output at which a signal OS is available which is linked to a node 10, and a second output, at which a first signal S1 which is to be tested is available, which is linked to a non-inverting input of a first amplifier LE1, and a third output, at which a second signal S2, which is to be tested is available, which is linked to a non-inverting input of a second amplifier LE2. Furthermore, the input of a signal output stage AS, for example an impedance amplifier, ~~is still linked to the node 10,~~ and at any one time a first negative input 20 and 30 of an AND logic gate L1 and L2 are additionally linked to the node 10. The output of the signal output stage AS is linked to the node 50, to which are linked, apart from the signal output OUT, a load resistor RL downstream of the voltage VDD and in each case the output of a voltage-controlled switching element E1 and a

voltage-controlled switching element E2. Furthermore, a first non-inverting input of a comparator I1 and a first non-inverting input of a comparator I2 are linked to the node 50. A lower threshold voltage V1 is available at the inverting input of the comparator I1, which together with the second upper threshold voltage V2 available at the inverting input of the comparator I2 forms a first voltage window discriminator. The output of the comparator I1 is linked to an affirmative input of an AND logic gate L1, and the output of the second comparator I2 is linked to a second negative input of ~~an~~ the AND logic gate L1. The output of the logic gage L1, at which a signal SE1 (MS) is available, is linked to both the control input of a switching element E1 and to the second input of the circuit unit SCH1. Furthermore, the node 50 is linked to a first non-inverting input of a comparator I3 and to a first non-inverting input of a comparator I4. A lower threshold voltage V3 is available at the inverting input of the comparator I3, which together with the upper threshold voltage V4 available at the inverting input of the comparator I4 forms a second voltage window discriminator. The output of the comparator I3 is linked to an affirmative input of an AND logic gage L2, and the output of the comparator I4 is linked to the second negative input of ~~an~~ the AND logic gate L2. The outlet of the logic gate L2, at which a signal SE2 is available, is linked to the control input of a ~~load~~ switching element E2. Furthermore, a reference voltage P1 is available at the inverting input of

the amplifier LE1. The output of the amplifier LE1, at which the signal SW1 is available, is linked to the node 50 ~~by means of~~ via the voltage-controlled switching element E1. Furthermore, a reference voltage P2 is available at the inverting input of the regulated amplifier LE2. The output of the amplifier LE2, at which the signal SW2 is available, is linked to the node 50 ~~by means of~~ via the voltage-controlled switching element E2.

Please insert a new paragraph at **page 8, at existing line 25**, as follows:

Figure 3 schematically shows the abovementioned varied embodiment with an integrated circuit IC having plural output pins OUT1, OUT2. While the defined potential value is applied to the first output pin OUT1 by the resistor W1 or W2 as described above, the signal SW1 or SW2 that is to be tested is provided at the second output pin OUT2.

[RESPONSE CONTINUES ON NEXT PAGE]